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10/708,365	02/26/2004	Jyi-Maw Hung	12036-US-PA	2364

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,365	HUNG ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2009 and 25 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8 and 20-32* is/are pending in the application.

4a) Of the above claim(s) *1,2,4-8 and 27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Applicant's election of ***Invention I (claims 20-26)*** in the reply filed on *22 December 2009* is acknowledged.

Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

3. ***Claims 27-32 are withdrawn*** from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on *22 December 2009*.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. *Claims 20-26* are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Independent claim 20 recites the subject matter: "*an operational amplifier having an inverting terminal coupled to a reference voltage, a non-inverting terminal coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and an output terminal coupled to a second terminal of the feedback resistor for outputting the Gamma voltage signal*" (see lines 9-12).

Such *operational amplifier terminal coupling* subject matter was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The original specification nowhere makes mention of inverting or non-inverting terminals.

And in light of the functionality of the gamma unit described in paragraph 28 of the original specification, it appears Figure 4 may have been mislabeled.

The Application appears to provide a "*Schmitt trigger*" with the functionality of a "*summing amplifier*" (*please see the provided Wikipedia documents*).

7. *Claims 20-26* are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Independent claim 20 recites the subject matter: "*an operational amplifier having an inverting terminal coupled to a reference voltage, a non-inverting terminal coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and an output terminal coupled to a second terminal of the feedback resistor for outputting the Gamma voltage signal*" (see lines 9-12).

Dependent claim 23 further recites the subject matter: "*the Gamma voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor*."

Such *operational amplifier terminal coupling* subject matter was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The original specification nowhere makes mention of inverting or non-inverting terminals.

And in light of the functionality of the gamma unit described in paragraph 28 of the original specification, it appears Figure 4 may have been mislabeled.

The Application appears to provide a "*Schmitt trigger*" with the functionality of a "*summing amplifier*" (*please see the provided Wikipedia documents*).

8. The remaining claims are rejected under 35 U.S.C. 112, first paragraph, as being dependent upon rejected base claims.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. *Claims 20-26* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claims 20 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter:

Independent claim 20 recites the subject matter: "*an operational amplifier having an inverting terminal coupled to a reference voltage, a non-inverting terminal coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and an output*

terminal coupled to a second terminal of the feedback resistor for outputting the Gamma voltage signal" (see lines 9-12).

Dependent claim 23 further recites the subject matter: "*the Gamma voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor*."

Claim 20 appears to describe a "*Schmitt trigger*"; and claim 23 provides it with the functionality of a "*summing amplifier*" (*please see the provided Wikipedia documents*).

As a result, it is unclear what kind of circuit the Applicant is attempting to claim.

The Applicant is respectfully requested to clarify what kind of circuit the Applicant is attempting to claim.

12. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

13. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. *Claims 20-26* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Clifton et al (US 6,388,648 B1)*** in view of the ***Instant Application's Admitted Prior Art (i.e., the APA)***, ***Liu (US 3,924,229 A)***, ***Suzuki (US 4,947,172 A)***, and ***Itoh (US 6,002,354 A)***.

Regarding Claim 20, ***Clifton*** discloses a circuit [*e.g., Fig. 14: color space converter circuit 180*] for generating a Gamma voltage signal [*e.g., Fig. 14: RGB_{OUT} voltage signals supplied as RGB input voltage signals to Fig. 9: gamma corrector 110*

-- wherein each RGB voltage signal is illustrated as the "S-curve" LCD characteristic response (Figs. 1AB: 2, Fig. 7: 90) prior to being converted into a "corrected curve" (Figs. 1AB: 6, Fig. 7: 92-99) --

which is to say, each RGB voltage signal (Fig. 14: RGB_{OUT}) is an "uncorrected" gamma voltage signal (Fig. 7: 90) that has yet to be converted by gamma corrector (Fig. 9: 110) into a "corrected" gamma voltage signal (Fig. 7: 92)],

the circuit being disposed on a ~~glass~~ substrate of a display panel [*e.g., Fig. 2: 12: Fig. 3: 40*],

the circuit comprising:

at least a first Gamma resistor [*e.g., Fig. 14: 1 kilohm resistor 186R*] having

a first terminal for receiving a first digital signal [*e.g., Fig. 14: buffered and inverted R signal output by buffer amplifier 182R*] and

a second terminal for outputting a first current [*e.g., Fig. 14: buffered and inverted R signal input to the non-inverting input of summing amplifier 188R*];

at least a second Gamma resistor [*e.g., Fig. 14: 10 kilohm resistor 210G, 100 kilohm resistor 212G*] having

a first terminal for receiving a second digital signal [*e.g., Fig. 14: buffered and inverted G signal output by buffer amplifier 182G*] and

a second terminal for outputting a second current [*e.g., Fig. 14: buffered and inverted G signal input to the non-inverting input of summing amplifier 188R*];

a feedback resistor [*e.g., Fig. 14: 1 kilohm feedback resistor 190R*] having

a first terminal coupled to the second terminal of the first Gamma resistor and the second terminal of the second Gamma resistor [*e.g., Fig. 14: coupled to the non-inverting input of summing amplifier 188R*]; and

an operational amplifier [*e.g., Fig. 14: summing amplifier 188R*] having

an inverting terminal [*e.g., Fig. 14: the "+" terminal -- please note that the "+" and "-" terminals of the summing amplifier 188R have been mislabeled/reversed in the illustration*] coupled to a reference voltage [*e.g., Fig. 14: electrical ground*],

a non-inverting terminal [*e.g., Fig. 14: the "-" terminal -- again, please note that the "+" and "-" terminals of the summing amplifier 188R have been mislabeled/reversed in the illustration*] coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and

an output terminal [*e.g., Fig. 14: summing amplifier 188R output terminal*] coupled to a second terminal of the feedback resistor for outputting the Gamma voltage signal,

wherein the Gamma voltage signal is determined by the first current, the second current and the feedback resistor

(*see the entire document, including Column 13, Line 57 - Column 15, Line 6*).

Firstly, ***Clifton's*** summing amplifier [*Fig. 14: 188R*] is illustrated with its "+" and "-" terminals mislabeled/reversed.

Clifton refers to the "-" terminal many times in the specification as "*the noninverting input of the summing amplifier 188*" (*e.g., see Column 14, Lines 16, 23, 29, 36, and 49*).

Secondly, even if it could be shown that the summing amplifier's terminals are not mislabeled/reversed, it would have been an obvious design choice to one having ordinary skill in the art at the time of invention to reverse the inputs to ***Clifton's*** summing amplifier [*Fig. 14: 188R*].

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., placing an operational amplifier in either an inverting or a noninverting configuration*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Thirdly, ***Clifton*** discloses the RGB values input into the color space converter circuit [*Fig. 14: 180*] as being "*analog signals*" -- whereas the instant claims are directed to first/second "*digital signals*."

It is noted here that an "*analog signal*" (i.e., a signal settable to two or more levels) inherently comprises a "*digital signal*" (i.e., a signal settable to two levels).

Moreover, ***Clifton*** discloses the RGB signals may take the form of "*fewer than 256 data values*" (*e.g., see Column 7, Line 59*).

Therefore, it would have been within ***Clifton's*** disclosed range for the RGB signals to only take two data levels.

Furthermore, ***Clifton's*** discloses the drive voltage taking values of both 0 and 1 whenever providing a black (*minimum luminance = 0*) and white (*maximum luminance = 1*) image for display (*e.g., see Figs. 1AB; Column 2, Lines 13-46*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to feed ***Clifton's*** color space converter circuit [*Fig. 14: 180*] with only "*0 and 1*" (*i.e., digital*) drive voltage levels when displaying a black-and-white, maximum contrast image.

Driving the display in such a black-&-white manner eliminates the need for gamma correction after the color space converter stage, because the uncorrected "*S-curve*" LCD characteristic response (*Figs. 1AB: 2, Fig. 7: 90*) coincides with the "*corrected curve*" (*Figs. 1AB: 6, Fig. 7: 92-99*) at such levels. Therefore, the RGB signals output by ***Clifton's*** color space converter circuit [*Fig. 14: 180*] at min/max voltage/luminance levels would actually be identical to the gamma voltages used by the display. And all of ***Clifton's*** display screens [*Fig. 2: 12A-12N*] would be perfectly matched.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., inputting "0 and 1" (i.e., digital) drive voltage levels when displaying a black-and-white, maximum contrast image*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Fourthly, ***Clifton's*** color space converter circuit [*Fig. 14: 180*] does indeed generate "*Gamma voltage signals*."

Fig. 14's RGB_{OUT} voltage signals are supplied as RGB input voltage signals to Fig. 9's gamma corrector (110). In order to have the gamma "*corrected*," it follows that the input signal must be a gamma signal (*albeit an "uncorrected" one*) to begin with.

Each RGB voltage signal is illustrated as the "*S-curve*" LCD characteristic response (*Figs. 1AB: 2, Fig. 7: 90*) prior to being converted into a "*corrected curve*" (*Figs. 1AB: 6, Fig. 7: 92-99*).

Therefore, each RGB voltage signal (*Fig. 14: RGB_{OUT}*) is an "*uncorrected*" gamma voltage signal (*Fig. 7: 90*) that has yet to be converted by gamma corrector (*Fig. 9: 110*) into a "corrected" gamma voltage signal (*Fig. 7: 92*).

It is additionally and respectfully noted that the instant application states, "*a Gamma circuit is necessary for voltage manipulation for image signal modification*" (see the last two lines of Paragraph 5 in the instant specification).

Clifton's color space converter circuit [*Fig. 14: 180*] does indeed provide "*voltage manipulation for image signal modification,*" as instantly disclosed.

Fifthly, ***Clifton*** does not expressly disclose the circuit being disposed on a glass substrate of a display panel.

However, the ***APA*** discloses disposing image driving circuitry [*e.g., Fig. 1a; 120*] and gamma circuitry [*e.g., Fig. 1a; 140*] on a glass substrate of a display panel [*e.g., Fig. 1a; 110*] for generating a Gamma voltage signal [*e.g., Fig. 1c; G*] (*e.g., see the entire **APA**, including Paragraphs 5-8*).

Clifton and the ***APA*** are analogous art, because they are from the shared inventive field of gamma circuitry for liquid crystal displays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the ***APA's*** gamma/driving-circuitry-on-glass arrangement with ***Clifton's*** circuitry, so as to provide a conventional gamma circuitry arrangement.

Sixthly, should it still be shown that the above cited prior art does not teach the circuit with sufficient specificity:

Liu discloses a digital-to-analog circuit [*e.g., Fig. 1*] for generating a voltage signal [*e.g., Fig. 1: at 26*],

the circuit comprising:

at least a first resistor [*e.g., Fig. 1: 14a = 1000 ohms*] having

a first terminal for receiving a first digital signal [*e.g., Fig. 1: reference potential via* S_1] and

a second terminal for outputting a first current;

at least a second resistor [*e.g., Fig. 1: 14b = 2000 ohms*] having

a first terminal for receiving a second digital signal [*e.g., Fig. 1: reference potential via* S_2] and

a second terminal for outputting a second current;

a feedback resistor [*e.g., Fig. 1: 12 = 1000 ohms*] having

a first terminal coupled to the second terminal of the first resistor and

the second terminal of the second resistor; and

an operational amplifier [*e.g., Fig. 1: 10*] having

a non-inverting terminal [*e.g., Fig. 1: 24*] coupled to a reference voltage [*e.g., Fig. 1:* E_R],

an inverting terminal [*e.g., Fig. 1: 22*] coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and

an output terminal [*e.g., Fig. 1: 26*] coupled to a second terminal of the feedback resistor for outputting the voltage signal,

wherein the voltage signal is determined by the first current, the second current and the feedback resistor (*see the entire document, including Column 3, Line 25 - Column 6, Line 25*).

Clifton and ***Liu*** are analogous art, because they are from the shared inventive field of digital to analog conversion circuitry.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Liu's*** digital-to-analog circuit [*e.g., Fig. 1*] as ***Clifton's*** digital-to-analog circuit [*e.g., Fig. 10: 102*], after having sent ***Clifton's*** Gamma voltage signal [*e.g., Fig. 14:* RGB_{OUT}] to ***Clifton's*** analog to digital converter [*e.g., Fig. 10: Analog RGB Input to ADC 120*] and gamma correction lookup table [*e.g., Fig. 10: 100*], so as to make use of a well known and commonly understood digital-to-analog circuit that is capable of operating at relatively high speed with a high degree of accuracy [*e.g.,* ***Liu:*** *Column 1, Lines 50-55*].

Wherein, again, it would have been an obvious design choice to one having ordinary skill in the art at the time of invention to reverse the inputs to ***Liu's*** operational amplifier [*e.g., Fig. 1: 10*].

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., placing an operational amplifier in either an inverting or a noninverting configuration*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Seventhly, should it still be shown that the above cited prior art does not teach the circuit with sufficient specificity:

Suzuki discloses a digital-to-analog circuit [*e.g., Fig. 1*] for generating a voltage signal [*e.g., Fig. 1: output*],

the circuit comprising:

at least a first resistor [*e.g., Fig. 1: 2R*] having

a first terminal for receiving a first digital signal [*e.g., Fig. 1: 10 via SW1*] and

a second terminal for outputting a first current;

at least a second resistor [*e.g., Fig. 1: 4R*] having

a first terminal for receiving a second digital signal [*e.g., Fig. 1: 10 via SW2*] and

a second terminal for outputting a second current;

a feedback resistor [*e.g., Fig. 1: R*] having

a first terminal coupled to the second terminal of the first resistor and

the second terminal of the second resistor; and

an operational amplifier [*e.g., Fig. 1: 12*] having

a non-inverting terminal [*e.g., Fig. 1: "+"*] coupled to a reference voltage [*e.g., Fig. 1: electrical ground*],

an inverting terminal [*e.g., Fig. 1: "-"*] coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and

an output terminal [*e.g., Fig. 1: output*] coupled to a second terminal of the feedback resistor for outputting the voltage signal,

wherein the voltage signal is determined by the first current, the second current and the feedback resistor (*see the entire document, including Column 1, Line 10 - Column 2, Line 15*).

Clifton and ***Suzuki*** are analogous art, because they are from the shared inventive field of digital to analog conversion circuitry.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Suzuki's*** digital-to-analog circuit [*e.g., Fig. 1*] as ***Clifton's*** digital-to-analog circuit [*e.g., Fig. 10: 102*], after having sent ***Clifton's*** Gamma voltage signal [*e.g., Fig. 14:* RGB_{OUT}] to ***Clifton's*** analog to digital converter [*e.g., Fig. 10: Analog RGB Input to ADC 120*] and gamma correction lookup table [*e.g., Fig. 10: 100*], so as to make use of a well known and commonly understood digital-to-analog circuit that is capable of operating at relatively high speed with a high degree of accuracy.

Wherein, again, it would have been an obvious design choice to one having ordinary skill in the art at the time of invention to reverse the inputs to ***Suzuki's*** operational amplifier [*e.g., Fig. 1: 10*].

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., placing an operational amplifier in either an inverting or a non-inverting configuration*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Eighthly, should it still be shown that the above cited prior art does not teach the circuit with sufficient specificity:

Itoh discloses a digital-to-analog circuit [*e.g., Fig. 1*] for generating a voltage signal [*e.g., Fig. 1: Vout*],

the circuit comprising:

at least a first resistor [*e.g., Fig. 1: R0 + R1*] having

a first terminal for receiving a first digital signal [*e.g., Fig. 1: Vcc via 12 & S2*] and

a second terminal for outputting a first current;

at least a second resistor [*e.g., Fig. 1: R0 + R1 + R2*] having

a first terminal for receiving a second digital signal [*e.g., Fig. 1: Vcc via 12 & S3*] and

a second terminal for outputting a second current;

a feedback resistor [*e.g., Fig. 1: R0*] having

a first terminal coupled [*e.g., Fig. 1: via S1*] to the second terminal of the first resistor and

the second terminal of the second resistor; and

an operational amplifier [*e.g., Fig. 1: 11*] having

an inverting terminal [*e.g., Fig. 1: "-"*] coupled to a reference voltage [*e.g., Fig. 1: VR*],

a non-inverting terminal [*e.g., Fig. 1: "+"*] coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and

an output terminal [*e.g., Fig. 1: Vout*] coupled to a second terminal of the feedback resistor for outputting the voltage signal,

wherein the voltage signal is determined by the first current, the second current and the feedback resistor (*see the entire document, including Column 1, Line 20 - Column 2, Line 16*).

Clifton and ***Itoh*** are analogous art, because they are from the shared inventive field of digital to analog conversion circuitry.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Itoh's*** digital-to-analog circuit [*e.g., Fig. 1*] as ***Clifton's*** digital-to-analog circuit [*e.g., Fig. 10: 102*], after having sent ***Clifton's*** Gamma voltage signal [*e.g., Fig. 14: RGB_{OUT}*] to ***Clifton's*** analog to digital converter [*e.g., Fig. 10: Analog RGB Input to ADC 120*] and gamma correction lookup table [*e.g., Fig. 10: 100*], so as to make use of a well known and commonly understood digital-to-analog circuit that is capable of operating at relatively high speed with a high degree of accuracy.

Regarding Claim 21, ***Clifton*** discloses a resistance value of the first Gamma resistor [*e.g., Fig. 14: 1 kilohm resistor 186R*] is equal to a resistance value of the feedback resistor [*e.g., Fig. 14: 1 kilohm feedback resistor 190R*] (*see the entire document, including Column 13, Lines 57-66*).

Liu discloses a resistance value of the first resistor is equal to a resistance value of the feedback resistor (*e.g., see Column 5, Lines 15-25*).

Regarding Claim 22, ***Clifton*** discloses a resistance value of the second Gamma resistor [*e.g., Fig. 14: 10 kilohm resistor 210G, 100 kilohm resistor 212G*] is a multiple of the resistance value of the first Gamma resistor [*e.g., Fig. 14: 1 kilohm resistor 186R*] (*see the entire document, including Column 13, Line 57 - Column 14, Line 33*).

Liu discloses a resistance value of the second resistor is a multiple of the resistance value of the first resistor (*e.g., see Column 5, Lines 15-25*).

Suzuki discloses a resistance value of the second resistor is a multiple of the resistance value of the first resistor (*see the entire document, including Column 1, Line 10 - Column 2, Line 15*).

Regarding Claim 23, ***Clifton*** discloses the Gamma voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor (*see the entire document, including Column 13, Line 57 - Column 15, Line 6*).

Liu discloses the voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor (*see the entire document, including Column 3, Line 25 - Column 6, Line 25*).

Suzuki discloses the voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor (*see the entire document, including*

Column 1, Line 10 - Column 2, Line 15 -- see also the provided Wikipedia entry for summing amplifiers).

Regarding Claim 24, ***Clifton*** discloses the reference voltage is a ground voltage (*see the entire document, including Fig. 14; Column 13, Line 57 - Column 15, Line 6*).

Suzuki discloses the reference voltage is a ground voltage (*see the entire document, including Column 1, Line 10 - Column 2, Line 15*).

Regarding Claim 25, ***Clifton*** discloses the circuit is applied to a driving circuit [*e.g., Fig. 9; 104*] for driving the display panel (*see the entire document, including Column 13, Line 57 - Column 15, Line 6*).

Regarding Claim 26, ***Clifton*** discloses the display panel is a liquid crystal display panel [*e.g., Fig. 2: 12: Fig. 3: 40*] (*see the entire document, including Column 13, Line 57 - Column 15, Line 6*).

Response to Arguments

17. Applicant's arguments filed on *25 May 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*Applicants respectfully submit that the connection relationship for the inverting and the non-inverting terminals of the operational amplifier of the present*

invention is different from ***Clifton****. To be specific, the inverting terminal of the operational amplifier of the present invention is coupled to a reference voltage such as the ground voltage, but the inverting terminal of* ***Clifton*** *is not coupled to the ground voltage (please see FIG. 14 of* ***Clifton****)*." (see Page 12 of the Response filed on *25 May 2009*). However, the examiner respectfully disagrees.

Clifton's summing amplifier [*Fig. 14: 188R*] is illustrated with its "+" and "-" terminals mislabeled/reversed.

Clifton refers to the "-" terminal multiple times in the specification as "*the noninverting input of the summing amplifier 188*" (*e.g., see Column 14, Lines 16, 23, 29, 36, and 49*).

Additionally, even if it were somehow shown that the summing amplifier's terminals are not mislabeled/reversed; it would have been an obvious design choice to one having ordinary skill in the art at the time of invention to reverse the inputs to ***Clifton's*** summing amplifier [*Fig. 14: 188R*].

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., placing an operational amplifier in either an inverting or a noninverting configuration*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Furthermore, independent claim 20 recites the subject matter: "*an operational amplifier having an inverting terminal coupled to a reference voltage, a non-inverting terminal coupled to the first terminal of the feedback resistor for receiving the first and the second currents, and an output terminal coupled to a second terminal of the feedback resistor for outputting the Gamma voltage signal*" (see lines 9-12).

Whereas, dependent claim 23 recites the subject matter: "*the Gamma voltage is equal to a sum of the first and the second currents multiplied by the resistance value of the feedback resistor.*"

Claim 20 appears to describe a "*Schmitt trigger*"; and claim 23 provides it with the functionality of a "*summing amplifier*" (*please see the provided Wikipedia documents*).

The original specification nowhere makes mention of inverting or non-inverting terminals.

And in light of the functionality of the gamma unit described in paragraph 28 of the original specification, it appears Figure 4 may have been mislabeled.

As a result, it is unclear what kind of circuit the Applicant is attempting to claim.

The Applicant is respectfully requested to clarify what kind of circuit the Applicant is attempting to claim.

The Applicant contends, "*In addition, one terminal of the first Gamma resistor of the present invention is used for receiving a first digital signal, and one terminal of the second Gamma resistor of the present invention is used for receiving a second digital signal. However,*

one terminal of the resistor 186R of ***Clifton*** *corresponding to the first Gamma resistor of the present invention is used for receiving an analog signal R rather than digital signal, and one terminal of the resistor 210G connecting in series with the resistor 212G of Clifton corresponding to the first Gamma resistor of the present invention is used for receiving an analog signal G rather than digital signal (please see column 13, lines 57-58 of* ***Clifton****)*." (see Page 12 of the Response filed on *25 May 2009*). However, the examiner respectfully disagrees.

Clifton discloses that the RGB values input into the color space converter circuit [*Fig. 14: 180*] are "*analog signals*" -- whereas the instant claims are directed to a first/second "*digital signals*."

It is noted that a set of "*analog signals*" (i.e., signals possessing two or more levels) inherently includes a set of "*digital signals*" (i.e., signals possessing two levels).

Moreover, ***Clifton*** discloses the RGB signals may take the form of "*fewer than 256 data values*" (*e.g., see Column 7, Line 59*).

Therefore, it would have been within ***Clifton's*** disclosed range for the RGB signals to only take two data levels.

Furthermore, ***Clifton's*** discloses the drive voltage taking values of both 0 and 1 whenever providing a black (*minimum luminance = 0*) and white (*maximum luminance = 1*) image for display (*e.g., see Figs. 1AB; Column 2, Lines 13-46*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to feed ***Clifton's*** color space converter circuit [*Fig. 14: 180*] with only "*0 and 1*" (*i.e., digital*) drive voltage levels when displaying a black-and-white, maximum contrast image.

Driving the display in such a black-&-white manner eliminates the need for gamma correction after the color space converter stage, because the uncorrected "*S-curve*" LCD characteristic response (*Figs. 1AB: 2, Fig. 7: 90*) coincides with the "*corrected curve*" (*Figs. 1AB: 6, Fig. 7: 92-99*) at such levels. Therefore, the RGB signals output by ***Clifton's*** color space converter circuit [*Fig. 14: 180*] at min/max voltage/luminance levels would actually be identical to the gamma voltages used by the display. And all of ***Clifton's*** display screens [*Fig. 2: 12A-12N*] would be perfectly matched.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*i.e., inputting "0 and 1" [i.e., digital] drive voltage levels when displaying a black-and-white, maximum contrast image*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

The Applicant contends, "*Furthermore, the technical efficiency of the circuit as claimed in the currently amended claim 20 is different from the analog color space converter circuit 180 of* ***Clifton***. *To be specific, the circuit as claimed in the currently amended claim 20 is used for generating Gamma voltage signal. However, the analog color space converter circuit 180 of* ***Clifton*** *is used for providing analog RGB output data (i.e. the primary color-corrected input information, please see* ***Clifton's*** *claim 1) rather than for generating Gamma voltage signal (please further see column 13, line 20 to column 14, line 65 of Clifton). Therefore, the analog color space converter circuit 180 of* ***Clifton*** *is not equivalent to the circuit as claimed in the*

currently amended claim 20" (see Page 12 of the Response filed on *25 May 2009*). However, the examiner respectfully disagrees.

Clifton's color space converter circuit [*Fig. 14: 180*] does indeed generate "*Gamma voltage signals*."

Figure 14's RGB_{OUT} voltage signals are supplied as RGB input voltage signals to Fig. 9's gamma corrector (110). In order to have their gamma "*corrected*," it follows that the input signals must be gamma signals (*albeit "uncorrected" ones*) to begin with.

Each RGB voltage signal is illustrated as the "*S-curve*" LCD characteristic response (*Figs. 1AB: 2, Fig. 7: 90*) prior to being converted into a "*corrected curve*" (*Figs. 1AB: 6, Fig. 7: 92-99*).

Therefore, each RGB voltage signal (*Fig. 14: RGB_{OUT}*) is an "*uncorrected*" gamma voltage signal (*Fig. 7: 90*) that has yet to be converted by gamma corrector (*Fig. 9: 110*) into a "*corrected*" gamma voltage signal (*Fig. 7: 92*).

It is additionally and respectfully noted that the instant application states, "*a Gamma circuit is necessary for voltage manipulation for image signal modification*" (see the last two lines of Paragraph 5 in the instant specification).

Clifton's color space converter circuit [*Fig. 14: 180*] does indeed provide "*voltage manipulation for image signal modification,*" as instantly disclosed.

Applicant's arguments with respect to *claims 20-26* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The documents listed on the attached '*Notice of References Cited*' are cited to further evidence the state of the art pertaining to generating gamma voltage signals.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
9 March 2010